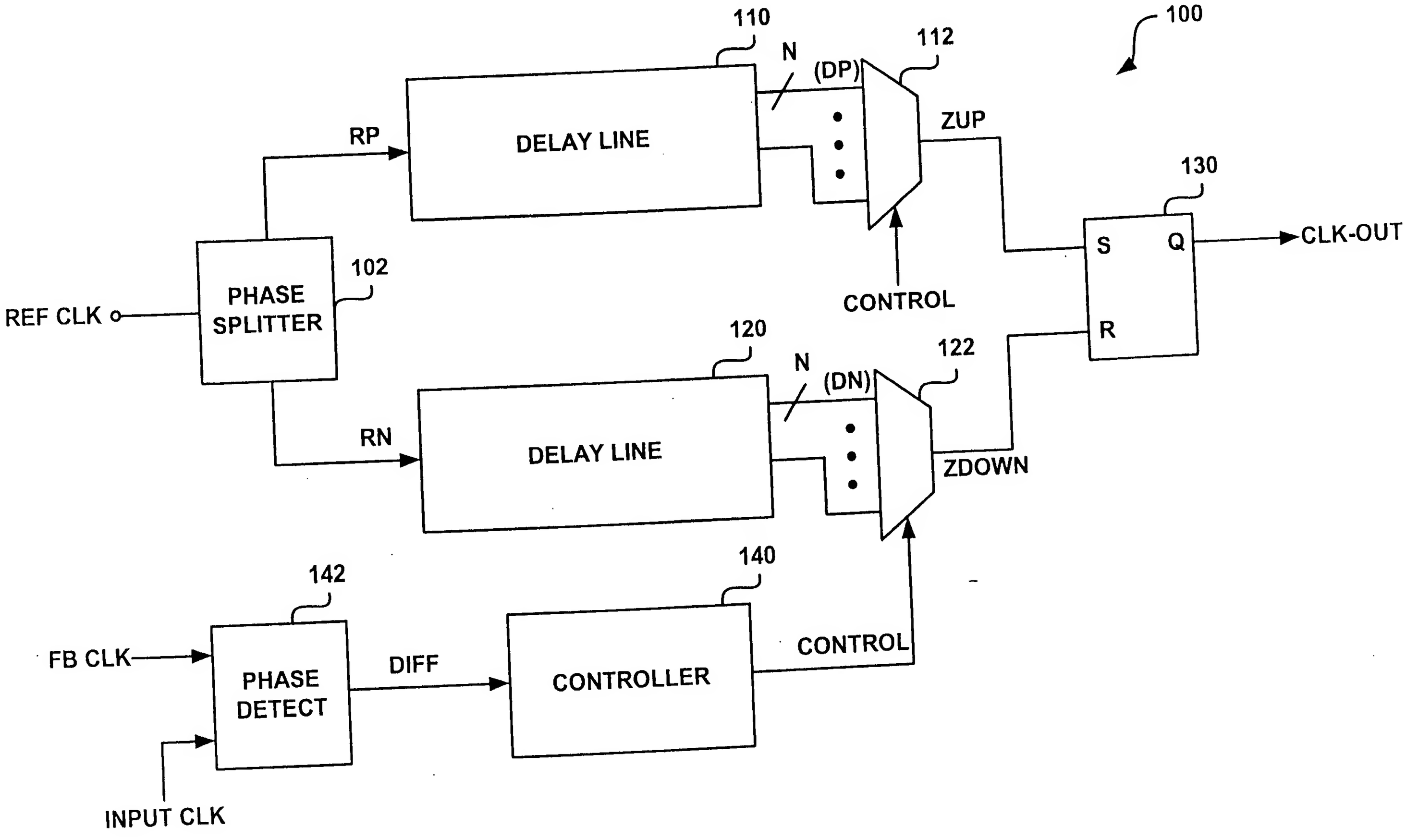
FIGURE 1


100
110
N
(DP)
112
RP
DELAY LINE
ZUP
130
S
Q
CLK-OUT
REF CLK
PHASE SPLITTER
102
CONTROL
R
120
N
(DN)
122
RN
DELAY LINE
ZDOWN
140
142
CONTROL
FB CLK
PHASE DETECT
DIFF
CONTROLLER
INPUT CLK

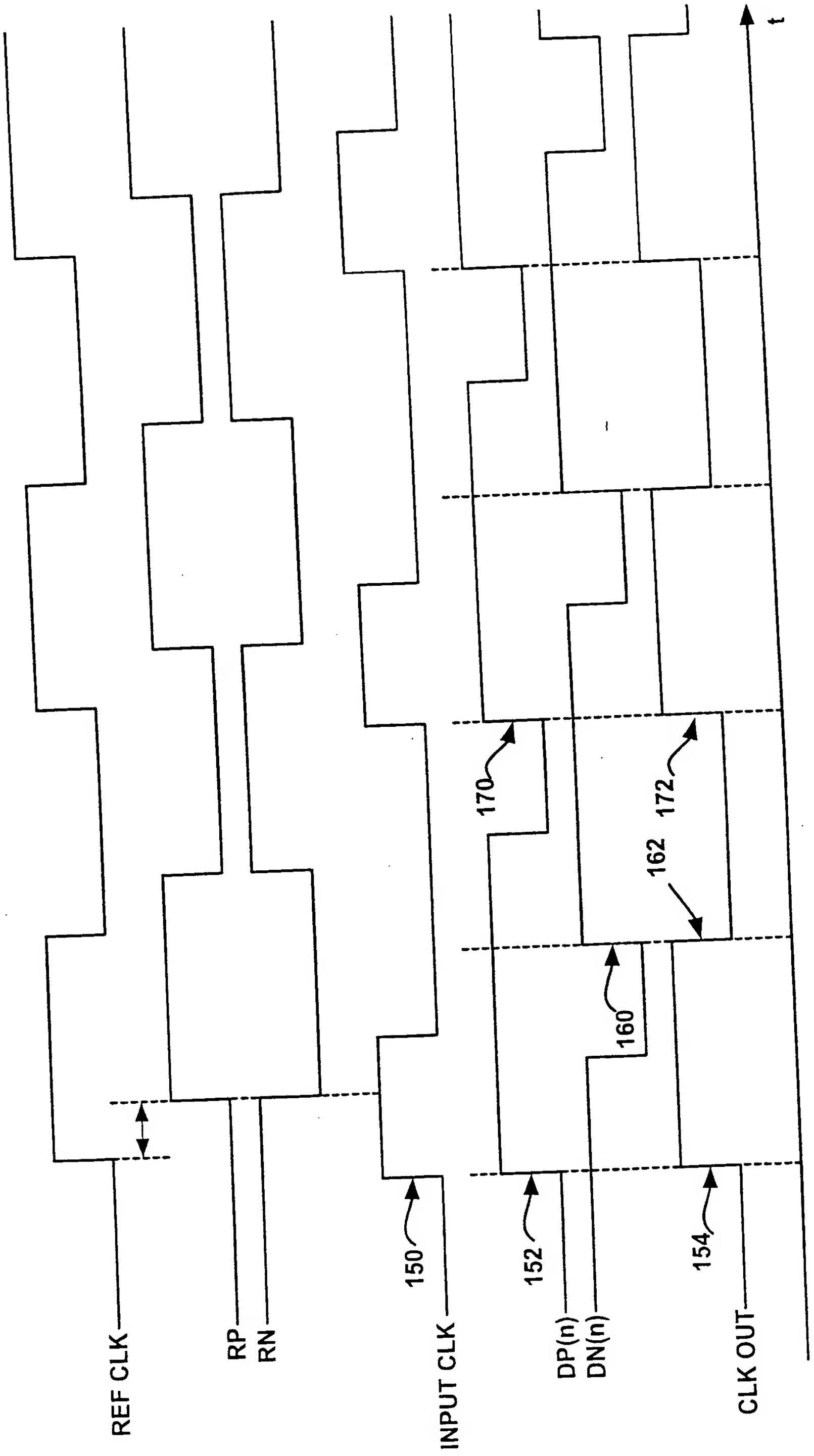

REF CLK
RP
RN
150
INPUT CLK
152
DP(n)
DN(n)
154
CLK OUT
160
162
170
172

FIGURE 2

FIGURE 3

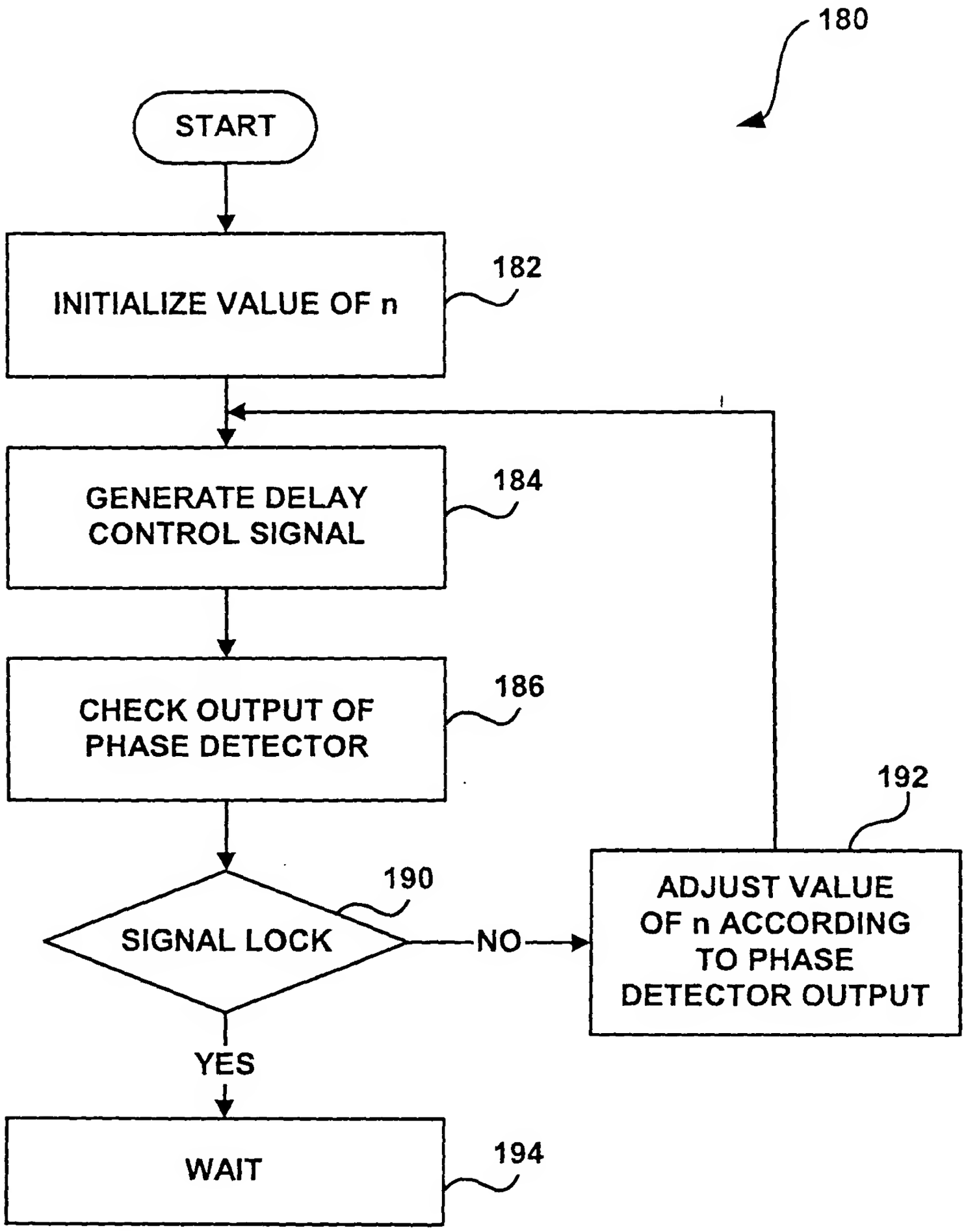

180
START
INITIALIZE VALUE OF n
182
GENERATE DELAY CONTROL SIGNAL
184
CHECK OUTPUT OF PHASE DETECTOR
186
SIGNAL LOCK
190
NO
ADJUST VALUE OF n ACCORDING TO PHASE DETECTOR OUTPUT
192
YES
WAIT
194

FIGURE 4

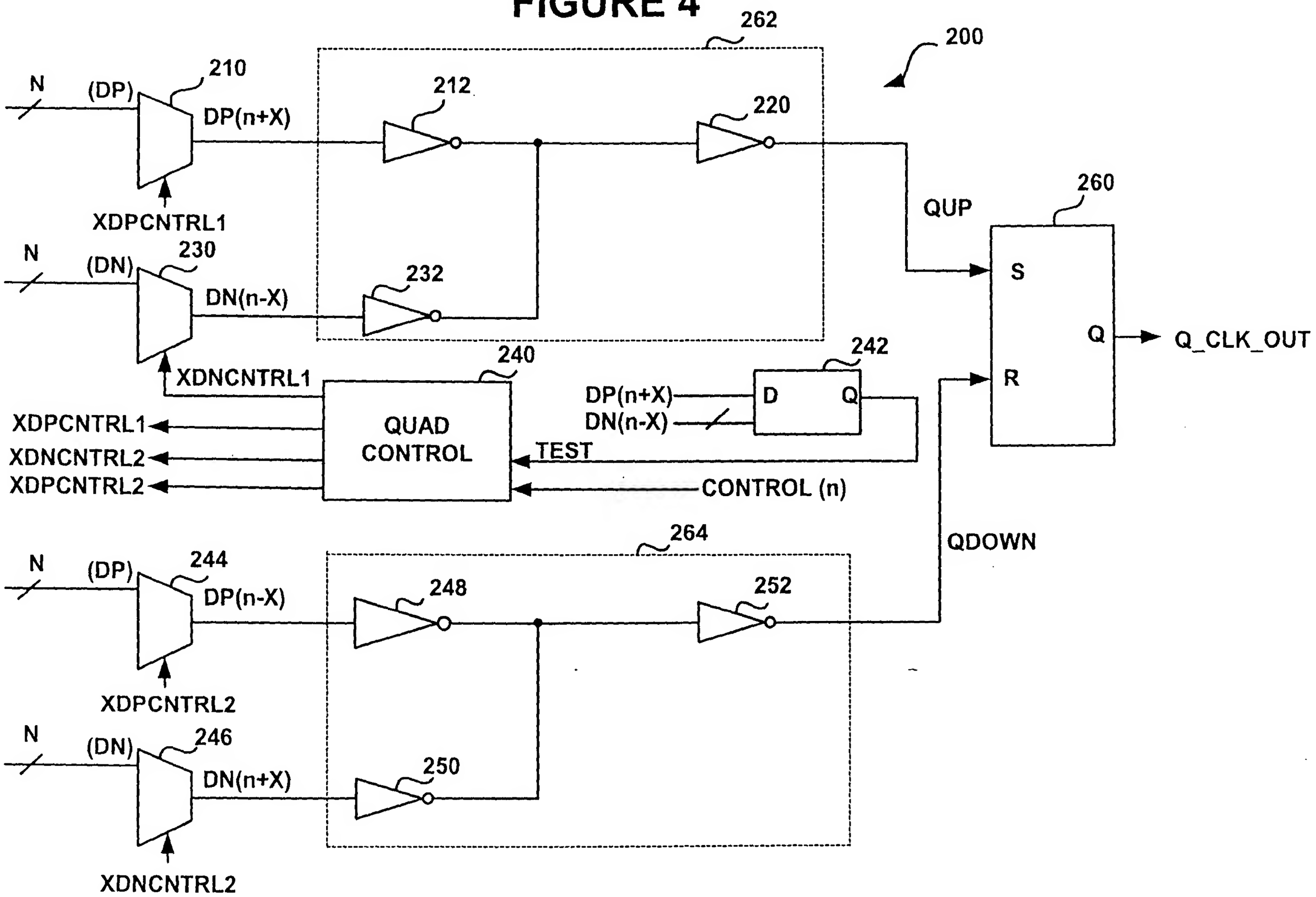

262
200
210
212
220
N
(DP)
DP(n+X)
XDPCNTRL1
QUP
260
230
N
(DN)
232
DN(n-X)
S
Q
Q_CLK_OUT
240
242
XDNCNTRL1
DP(n+X)
D
Q
XDPCNTRL1
QUAD
CONTROL
DN(n-X)
R
XDNCNTRL2
TEST
XDPCNTRL2
CONTROL (n)
QDOWN
264
244
N
(DP)
248
252
DP(n-X)
XDPCNTRL2
246
N
(DN)
250
DN(n+X)
XDNCNTRL2

FIGURE 5

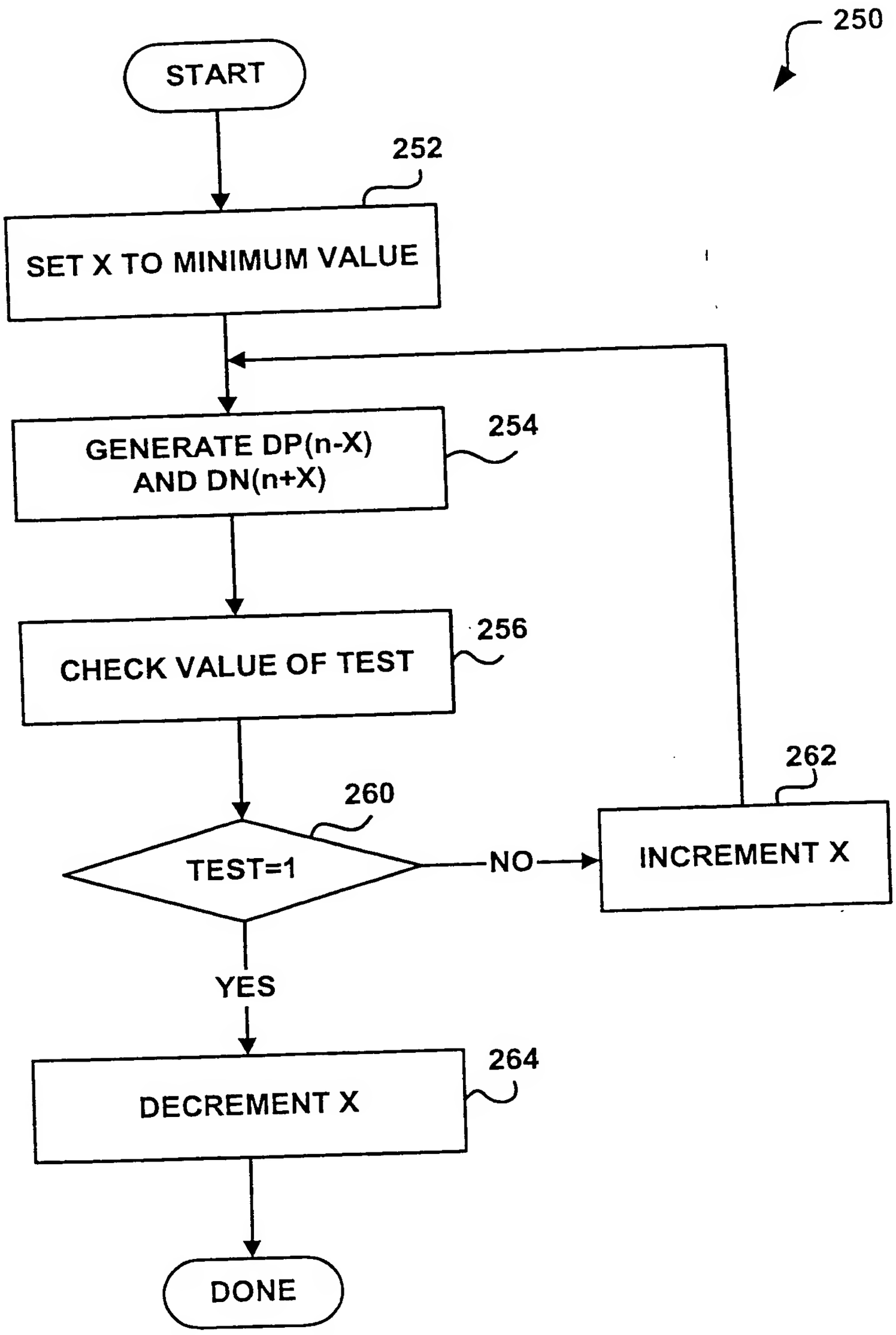

250
START
252
SET X TO MINIMUM VALUE
254
GENERATE DP(n-X)
AND DN(n+X)
256
CHECK VALUE OF TEST
260
TEST=1
NO
262
INCREMENT X
YES
264
DECREMENT X
DONE

FIGURE 6

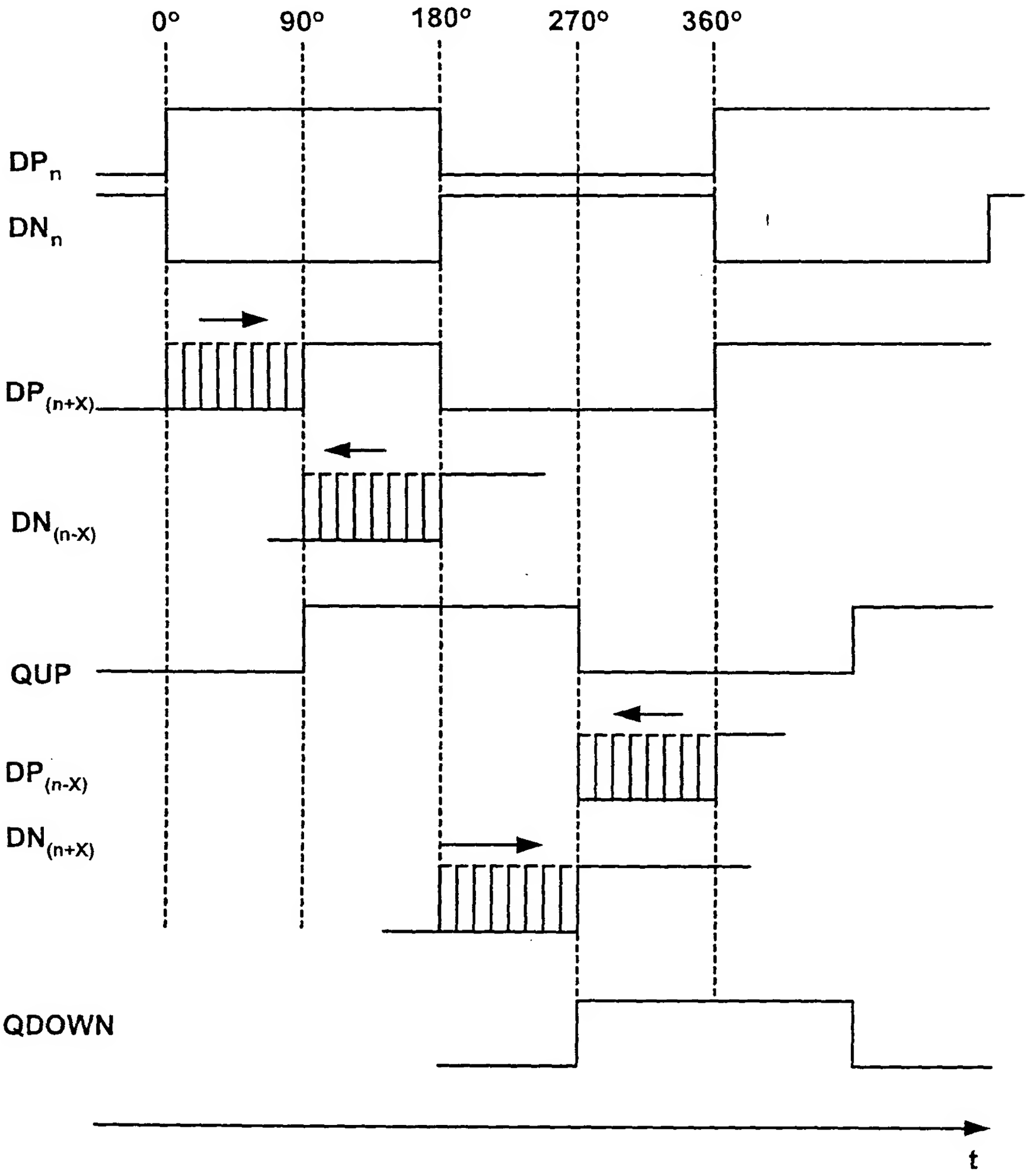


FIGURE 7

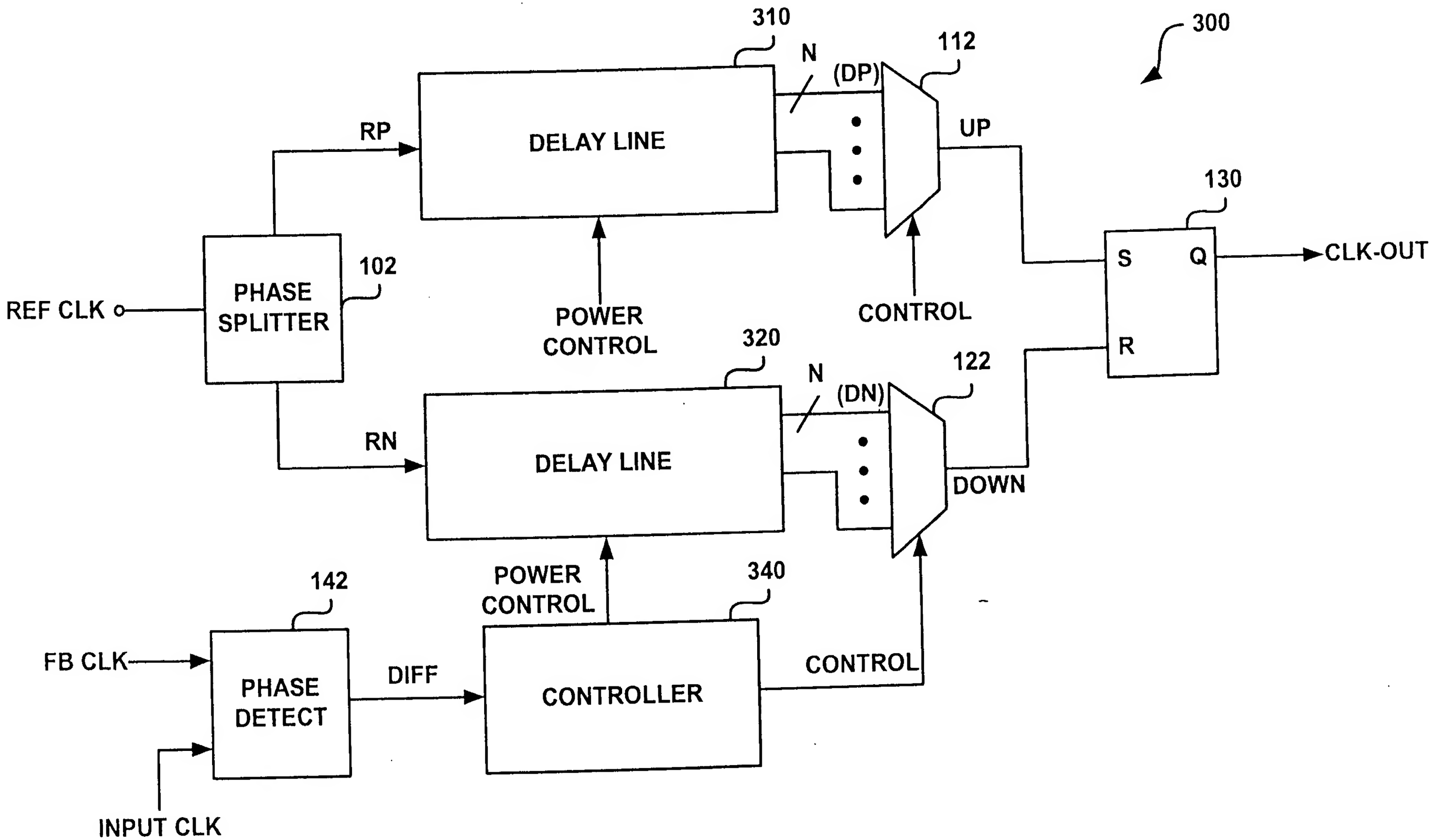

300
310
N
(DP)
112
RP
DELAY LINE
UP
130
S
Q
CLK-OUT
REF CLK
102
PHASE SPLITTER
POWER CONTROL
CONTROL
R
320
122
N
(DN)
RN
DELAY LINE
DOWN
142
POWER CONTROL
340
FB CLK
PHASE DETECT
DIFF
CONTROLLER
CONTROL
INPUT CLK

FIGURE 8

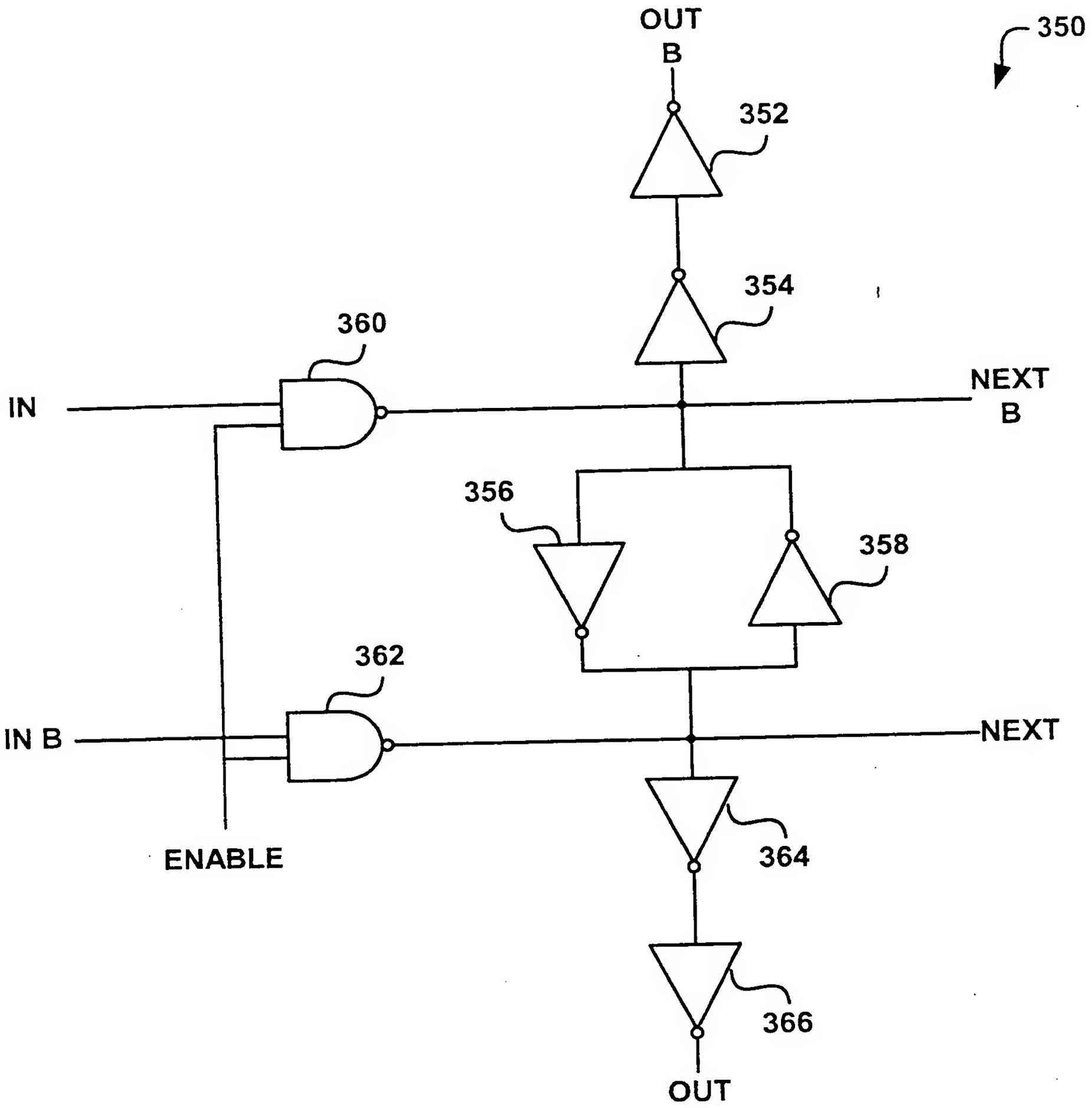

OUT
B
350
352
354
360
IN
NEXT
B
356
358
362
IN B
NEXT
ENABLE
364
366
OUT

FIGURE 9

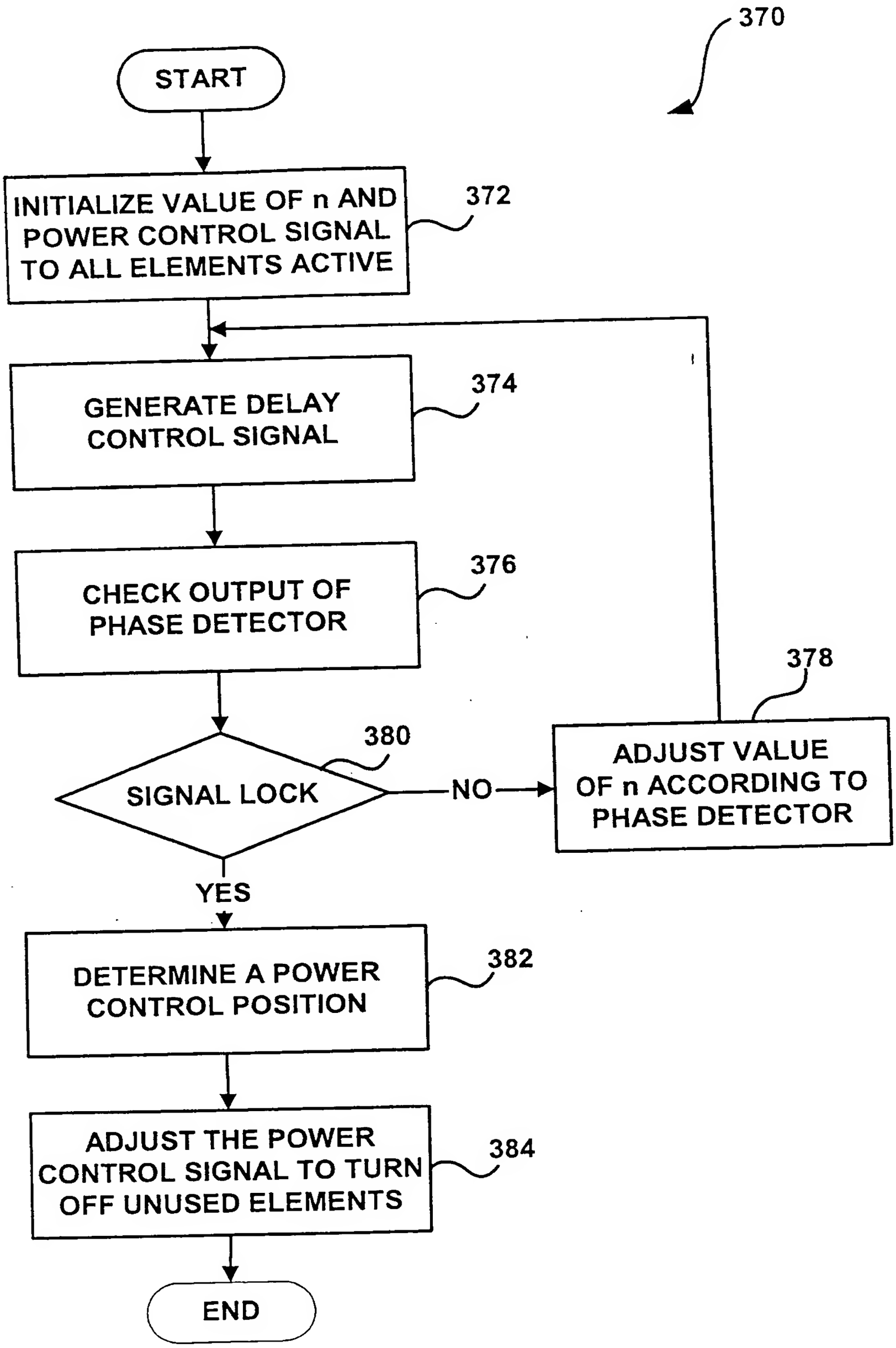

370
START
INITIALIZE VALUE OF n AND POWER CONTROL SIGNAL TO ALL ELEMENTS ACTIVE
372
GENERATE DELAY CONTROL SIGNAL
374
CHECK OUTPUT OF PHASE DETECTOR
376
SIGNAL LOCK
380
NO
ADJUST VALUE OF n ACCORDING TO PHASE DETECTOR
378
YES
DETERMINE A POWER CONTROL POSITION
382
ADJUST THE POWER CONTROL SIGNAL TO TURN OFF UNUSED ELEMENTS
384
END

FIGURE 10

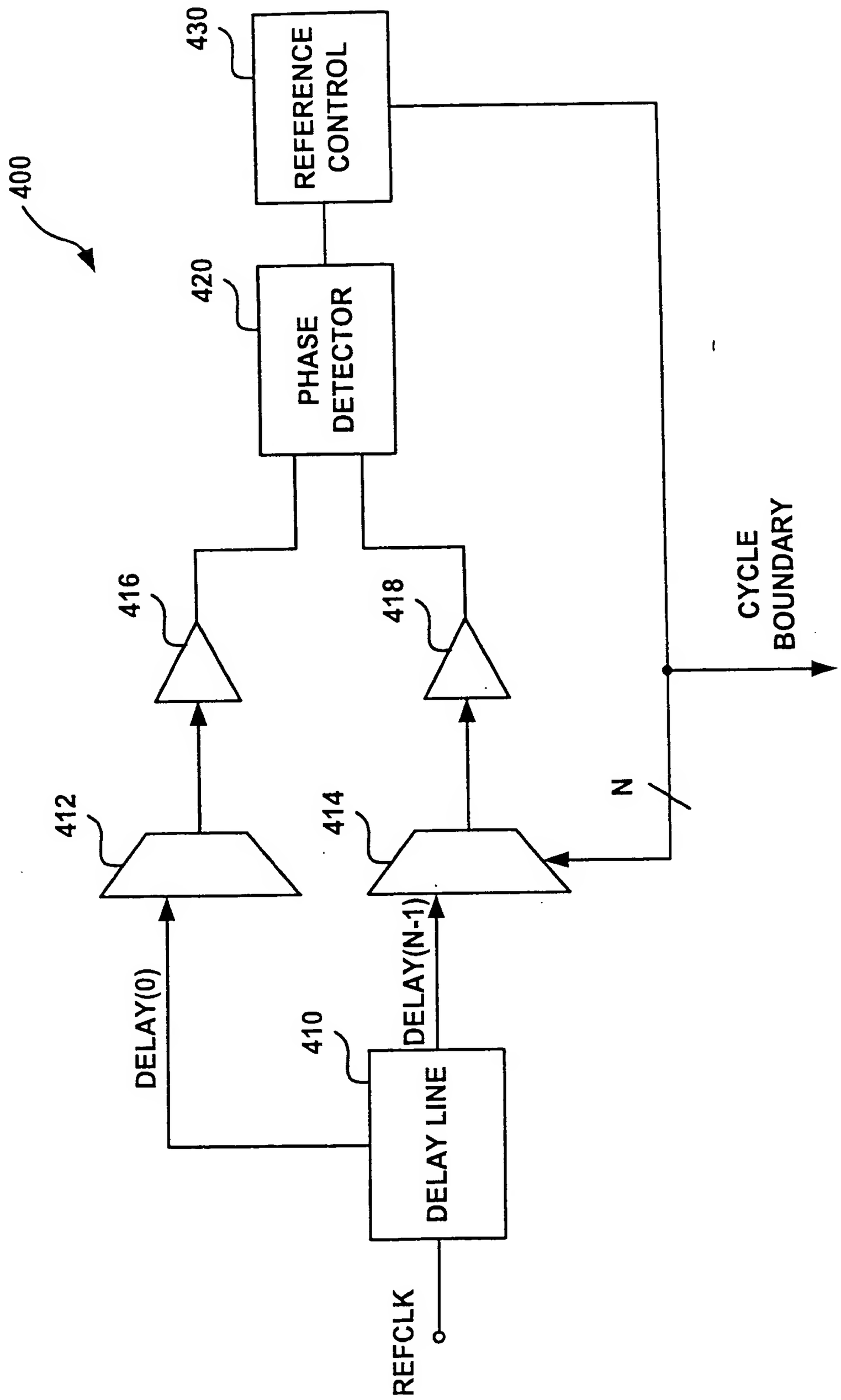

400
430
REFERENCE CONTROL
420
PHASE DETECTOR
416
418
CYCLE BOUNDARY
412
414
N
DELAY(0)
DELAY(N-1)
410
DELAY LINE
REFCLK

FIGURE 11

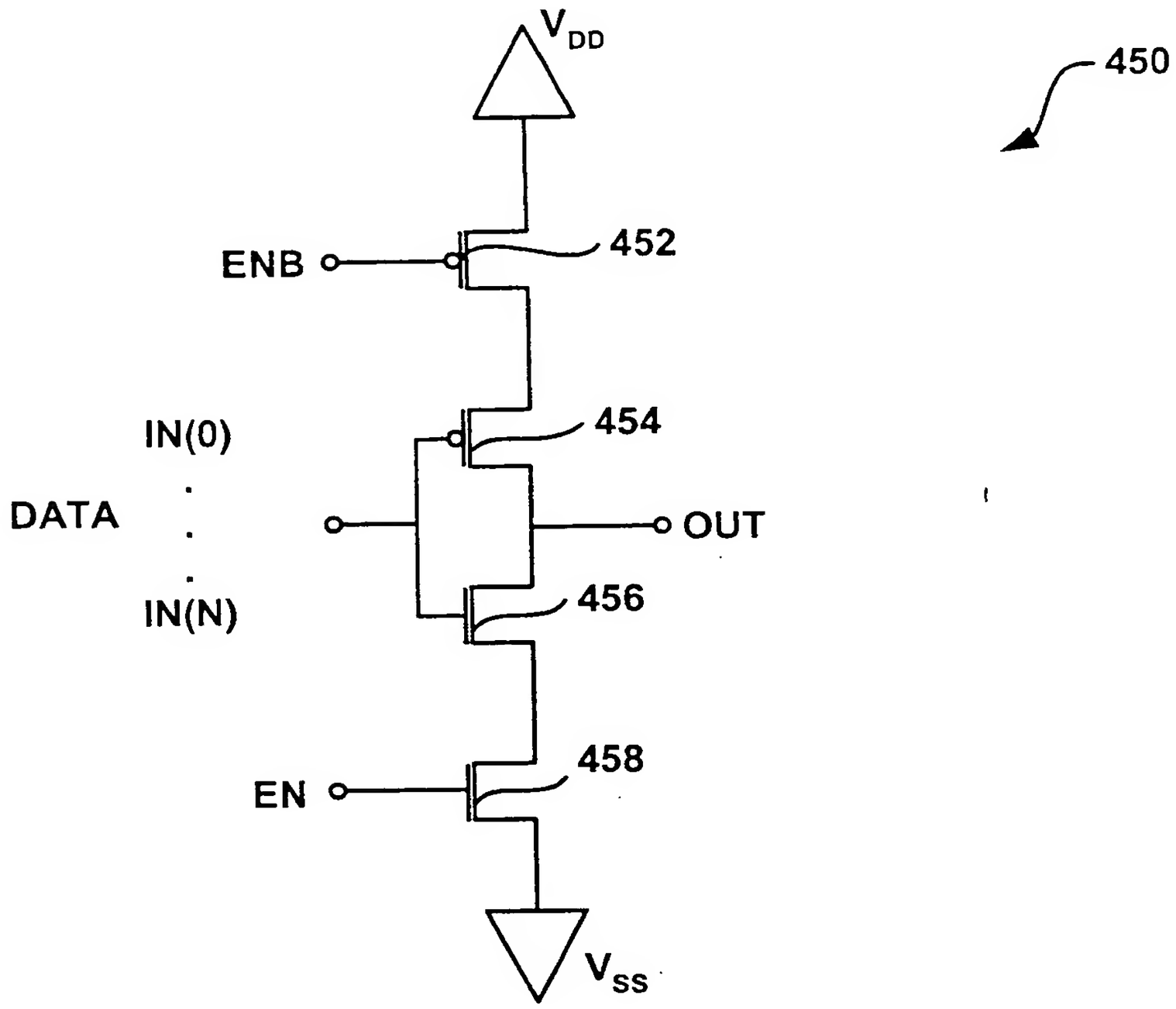


FIGURE 12

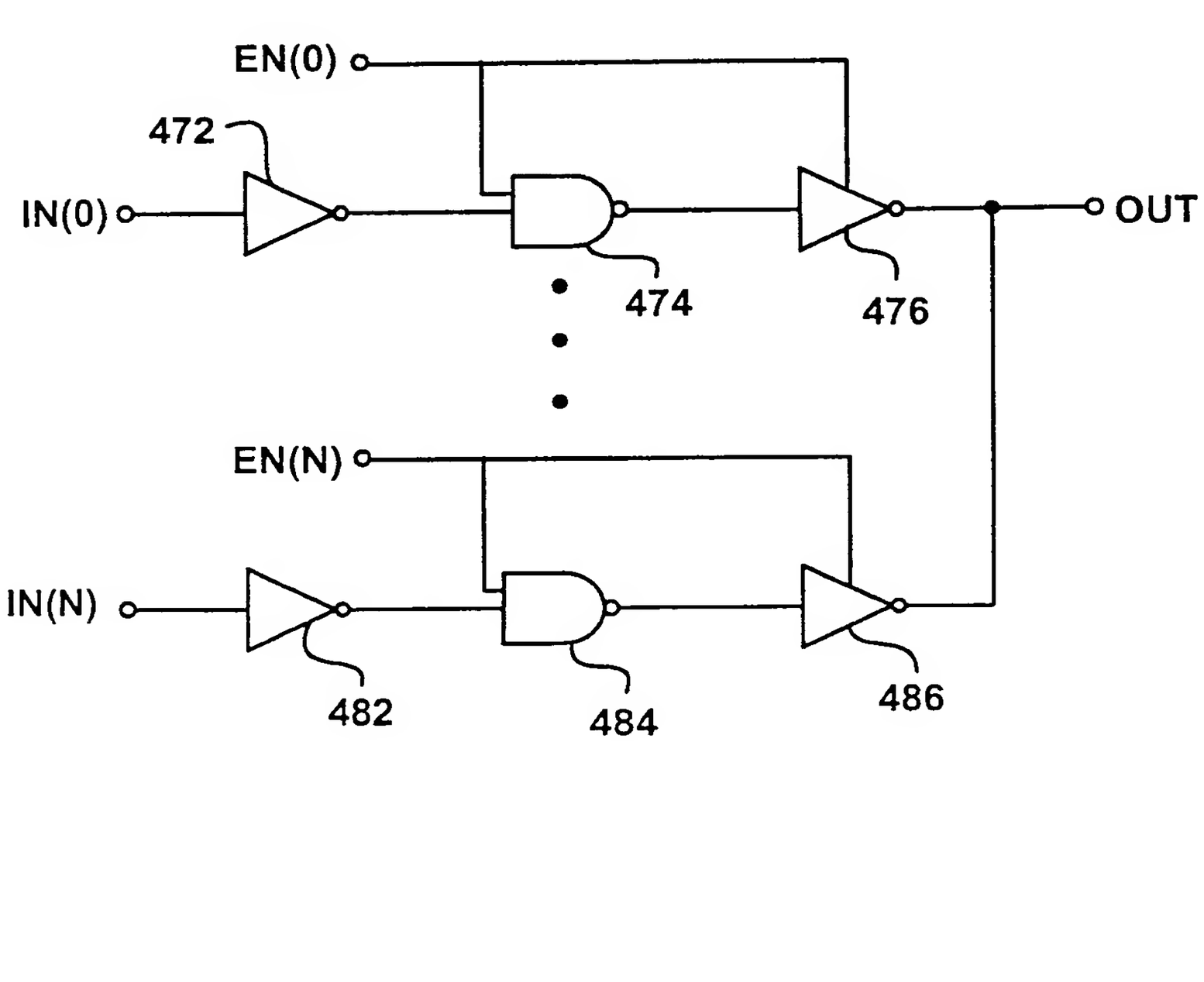
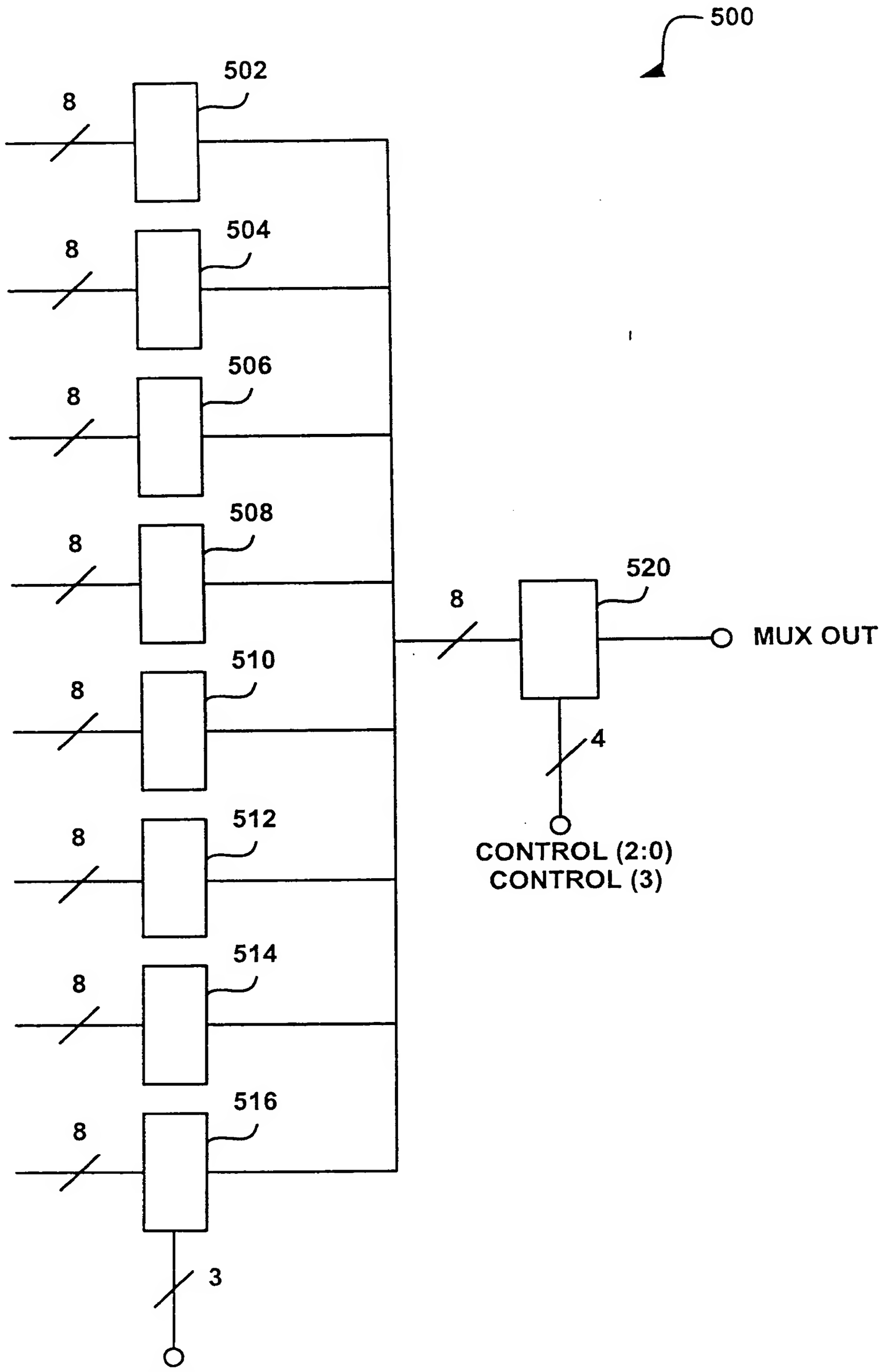


FIGURE 13


500
502
8
504
8
506
8
508
8
510
8
512
8
514
8
516
8
520
8
MUX OUT
4
CONTROL (2:0)
CONTROL (3)
3
CONTROL (5:3)

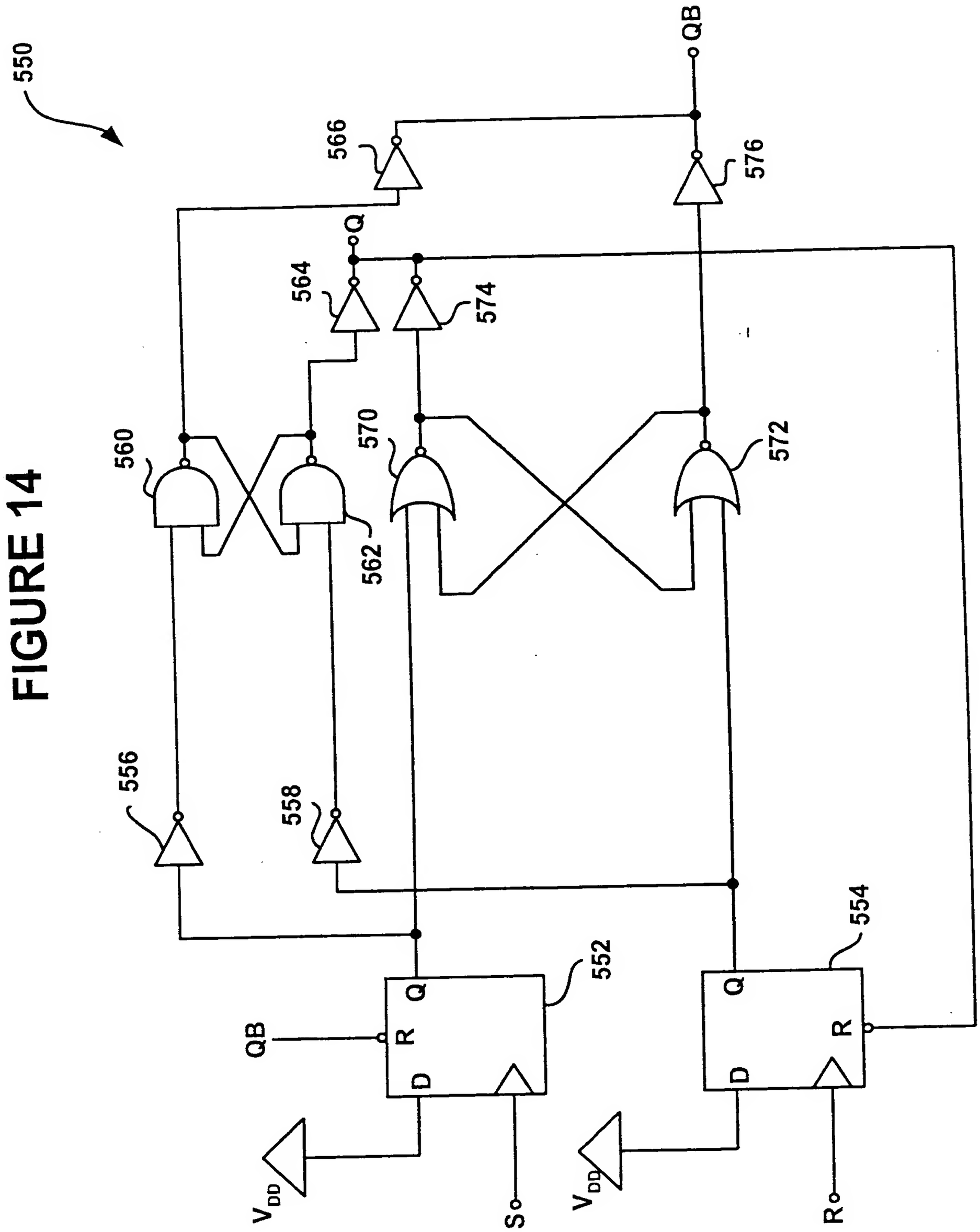

550
QB
566
576
Q
564
574
560
570
572
562
556
558
554
552
Q
R
D
QB
V_{DD}
S
Q
R
D
V_{DD}
R

FIGURE 14